ABSTRACT

A method is described to fabricate a MOSFET device with increased threshold voltage stability. After the pad oxide and pad nitride are deposited on the silicon substrate and shallow trenches are patterned and the pad nitride removed. As^+ or P^+ species are then implanted using low energy ions of approximately 5 keV into the pad oxide. Conventional As^+ or P^+ implant follows the shallow implant to form the n- wells. With this procedure of forming a sacrificial shallow implantation oxide layer, surface dopant concentration variation at pad oxide:silicon substrate interface is minimized; and threshold voltage stability variation of the device is significantly decreased.